



Systems Architecture

GCSE Student Booster

Key Information

- 1) Remember this booster is here to **help you**. Please consider your behaviour in the chat.
- 2) If you are in a room with a teacher/group, please login to the meeting. This is so we can mark your attendance. This information goes into a **prize draw**.
- 3) Make sure the name on the meeting is the **SAME** as the name on your Isaac account. We can't mark you present if they don't match.



Welcome

- What registers can you name that are within the processor?

- Add your answers to the chat
- 2 minutes



Intended Learning Outcomes

By the end of this session, you will be able to:

- Identify the sections of the von Neumann Architecture
- Explain how the fetch – decode – execute cycle is used in the CPU
- Discuss the factors that can affect the performance of the CPU
- Identify the difference between RAM and ROM

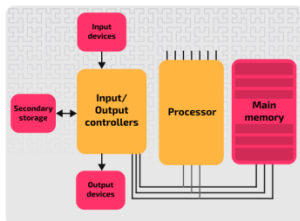


John von Neumann

- Hungarian-American mathematician, physicist and polymath.
- 1940's John von Neumann and his team developed the stored program computer.



Von Neumann Architecture



The Von Neumann architecture used the idea of **storing program instructions and data in main memory** and moving them between memory and the processor.



Von Neumann Architecture consists of:

- a **processor**
- a **memory unit** that can communicate directly with the processor
- connections for **input and output** devices
- **secondary storage** for saving/backing up data



The Processor

- Responsible for **executing the instructions** of programs.
- Made up of **several important components**, each of which has a **specific role**.
- These are the **Control Unit**, the **Arithmetic & Logic Unit** and **Registers**.



Control Unit

- **Controls the flow of data** around the CPU.
- It does this through the use of **control signals** that allow the processor to read from/write to main memory.
- Responsible for **decoding instructions**.



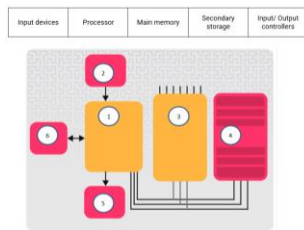
Arithmetic and Logic Unit

- Responsible for **performing arithmetic calculations** and **logical operations** that include:
 - Addition, subtraction, multiplication, division
 - Logical operations (e.g. AND, OR, NOT)
 - Comparisons between values (greater than, less than, equal to)
 - Shifting binary patterns to the left or right



Handout 1 Task 1

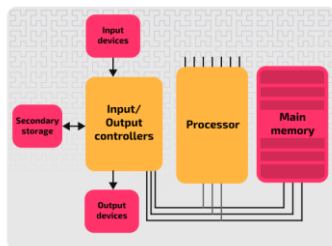
- Use the diagram and label the different sections of the von Neumann architecture.
- Complete the fill in the gaps sentence.



5 minutes to complete



Handout 1 Task 1 - solution



The Von Neumann architecture used the idea of storing **program instructions** and **data** in **main memory** and moving them between memory and the processor.



Registers

Registers are locations of computer memory within the processor.

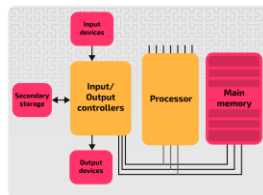
They are small and provide extremely fast access.

They are used to temporarily store data.



Buses

A bus is a collection of wires, through which data and signals are transmitted from one component to another.



Registers

Handout 1

Use **Handout 1** to make a note of the different acronyms and their meanings.

- **MAR** = Memory Address Register
- **MDR** = Memory Data Register
- **ACC** = Accumulator
- **PC** = Program Counter



Registers explained

Register	Purpose
Memory address register (MAR)	Holds the address of the instruction/data to be fetched from memory.
Memory data register (MDR)	Temporarily holds the data (data values or instructions) that are read from or written to the main memory
Program counter (PC)	Holds the address of the <u>next</u> instruction to be executed by the processor
Accumulator(ACC)	Stores the result of any calculation from ALU.



The von Neumann architecture

- CPU runs programs stored in memory.
- Data and instructions for programs are stored in memory addresses.
- Dedicated connections are used called **buses**



Buses



Address bus
identifies
address location



Data bus
transfers content
to/from locations



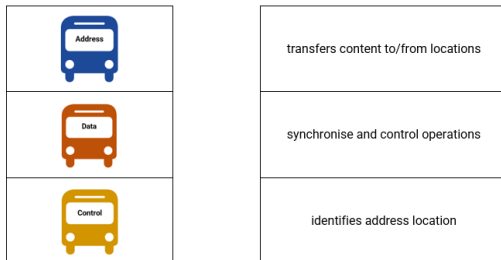
Control bus to
synchronise and
control operations



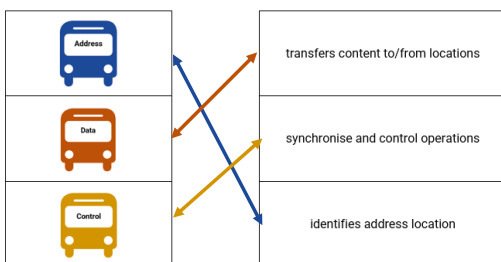
Handout 1

Handout 1 Task 2

- Match the correct bus and description



Handout 1 Task 2 – solution



Question

- Which one of these is a feature of the von Neumann architecture?

- Both data and instructions are stored together in main memory
- Only instructions are stored in main memory
- Only data is stored in main memory

Answers in the chat

Question

- Which one of these is a feature of the von Neumann architecture?

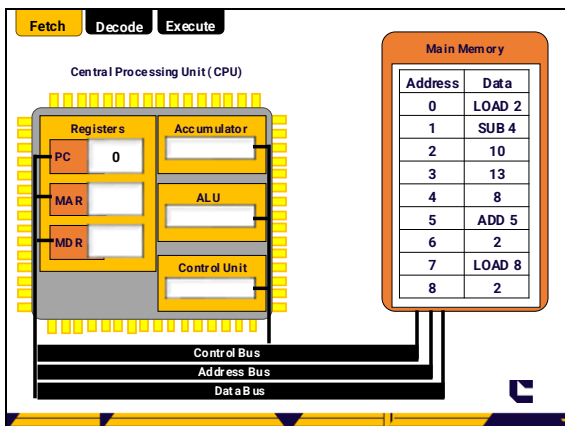
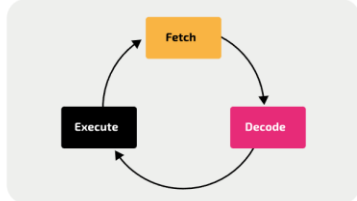
- A. Both data and instructions are stored together in main memory
- B. Only instructions are stored in main memory
- C. Only data is stored in main memory

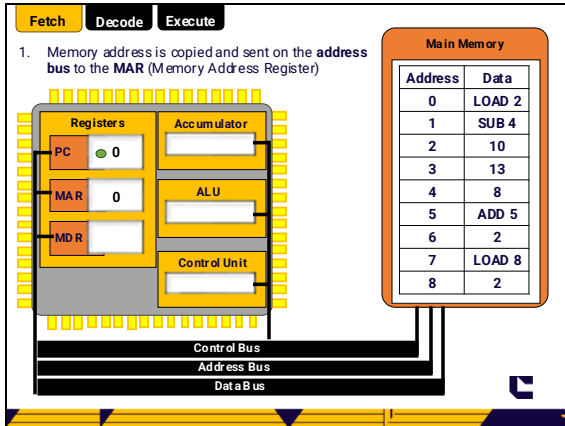
Answers in the chat

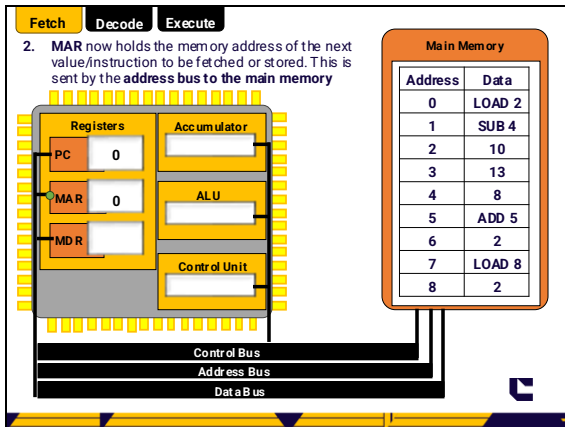


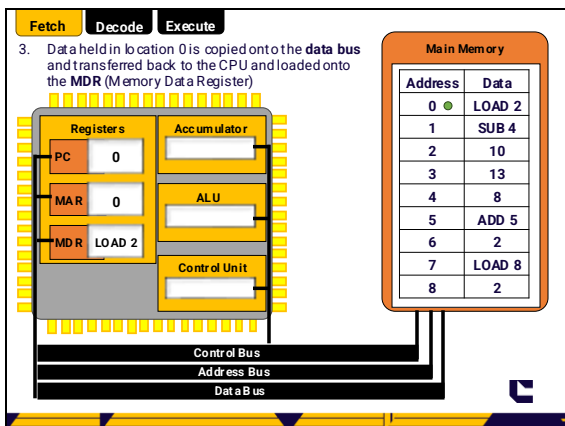
FDE Cycle

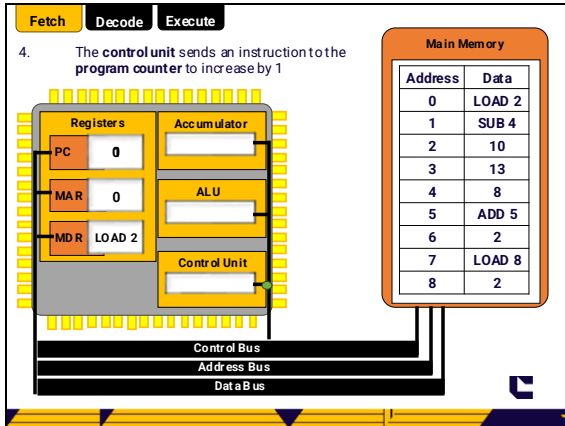
- A processor needs to use the **Fetch – Decode – Execute Cycle**











Handout 2 Task 1

Handout 2

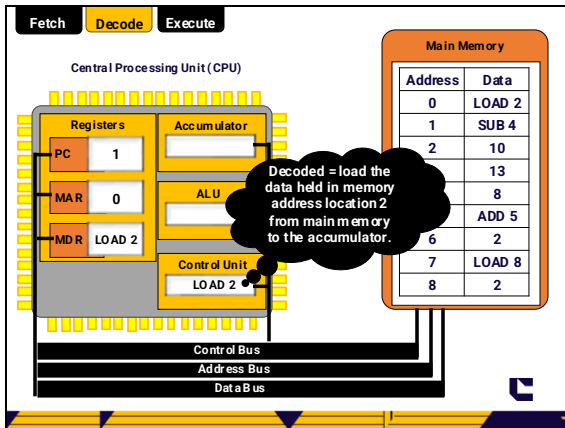
Using numbers identify the correct order of steps for the **Fetch** section of the cycle?

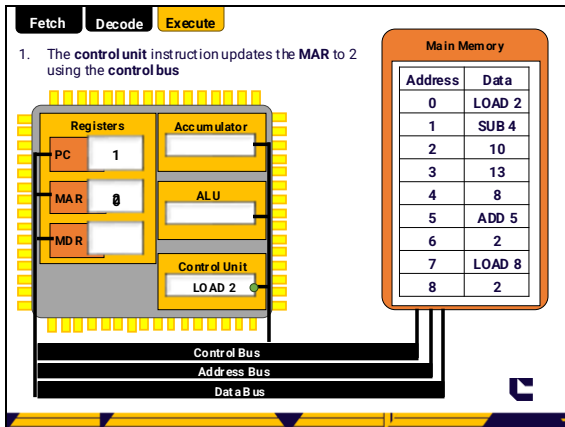
STEP order	Instruction
	Data held in location 0 is copied onto the data bus and transferred back to the CPU and loaded onto the MDR (Memory Data Register)
	The control unit sends an instruction to the program counter to increase by 1
	MAR now holds the memory address of the next value/instruction to be fetched or stored. This is sent by the address bus to the main memory
	Memory address is copied and sent on the address bus to the MAR (Memory Address Register)

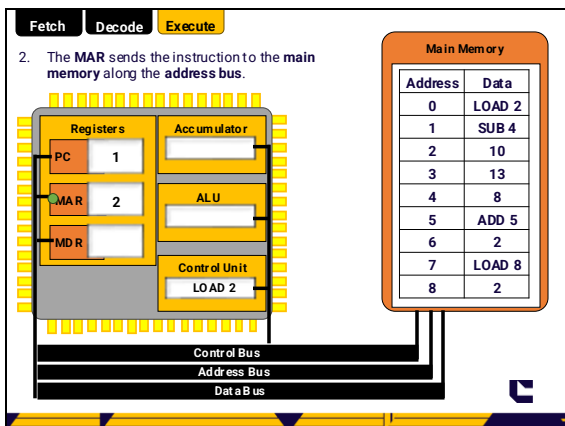
Handout 2 Task 1 – solution

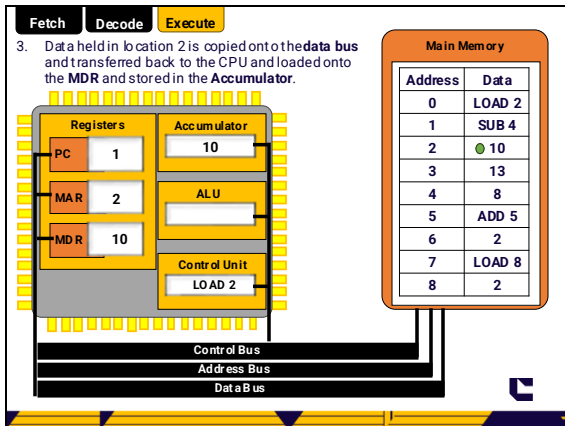
Using numbers identify the correct order of steps for the **Fetch** section of the cycle?

STEP order	Instruction
3	Data held in location 0 is copied onto the data bus and transferred back to the CPU and loaded onto the MDR (Memory Data Register)
4	The control unit sends an instruction to the program counter to increase by 1
2	MAR now holds the memory address of the next value/instruction to be fetched or stored. This is sent by the address bus to the main memory.
1	Memory address is copied and sent on the address bus to the MAR (Memory Address Register)









Handout 2 Task 2

Handout 2

Using numbers identify the correct order of steps for the **Execute** section of the cycle?

STEP order	Instruction
	The MAR sends the instruction to the main memory along the address bus.
	The control unit instruction updates the MAR to 2 using the control bus
	Data held in location 2 is copied onto the data bus and transferred back to the CPU and loaded onto the MDR and stored in the Accumulator.

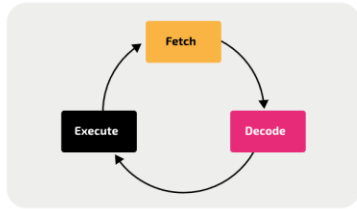
Handout 2 Task 2 – solution

Using numbers identify the correct order of steps for the **Execute** section of the cycle?

STEP order	Instruction
2	The MAR sends the instruction to the main memory along the address bus.
1	The control unit instruction updates the MAR to 2 using the control bus
3	Data held in location 2 is copied onto the data bus and transferred back to the CPU and loaded onto the MDR and stored in the Accumulator.

The cycle continues ...

- Moving through all instructions in order.



Game board 1

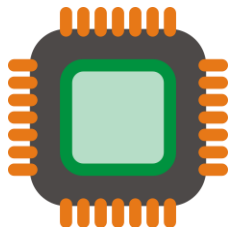
- <https://isaaccs.org/assignment/7c86fd9f-9c02-4cea-b009-33825dbf7c13>

5 minutes to complete



Factors affecting processor performance

- Cache
- Number of Cores
- Clock speed



Cache

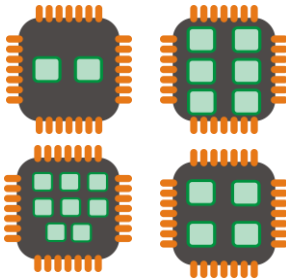
- High speed memory
- Close to or on the CPU
- Stores instructions and data frequently/commonly used.
- By having more cache we can store more instructions/data, and this saves us fetching it from RAM which is slower.



Handout 3 – Task 1

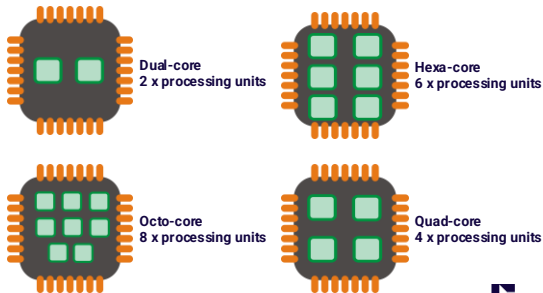
Handout 3

Match the diagram to the correct name and number of cores.
3 minutes

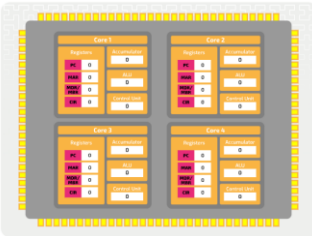


Handout 3 – Task 1 – solution

Match the diagram to the correct name and number of cores.



Number of cores



- Generally, more cores = more instructions the CPU can execute at once.
- However, doubling the cores does not double the speed!



Clock speed

- Processors are measured in clock speed – measured in GHz (gigahertz)
- 3.6GHz = 3.6 billion FDE cycles **per second**



Game board 2

- <https://isaacacs.org/assignment/0e7829b1-5c95-4be6-9b33-1751f12a2d32>

5 minutes to complete



Exam style question: discussion



- Compare and contrast the impact of increasing clock speed and adding more cores on CPU performance.
- In which scenarios would each approach be more beneficial?

Reflect upon the above for 2 minutes.



Main memory

- Accessed directly by the processor

	RAM	Random Access Memory
	ROM	Read Only Memory



Two types of memory

• Volatile

When power is no longer available anything stored on here is deleted.

• Non-volatile

Anything stored stays on there with and without power



RAM or ROM?

Answer in the chat

- Volatile
- Stores data and instructions currently in use
- Main memory
- Addressable locations
- Most often higher capacity

1

- Non – Volatile
- Permanent memory
- Stores BIOS

2



RAM

Random Access Memory

- Volatile
- Stores data and instructions currently in use
- Main memory
- Addressable locations



ROM

Read Only Memory

- Non – Volatile
- Permanent memory
- Stores BIOS



Final questions

- Which one of the following components is used to reduce how long the processor has to wait for data and instructions?

- A. Cache
- B. Bus
- C. ALU
- D. CU



Final questions

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- A. Cache
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Final questions

- Which parts of a computer program are held in RAM while it is processing?

- A. Only the instructions
- B. Instructions and data
- C. Only the data



Final questions

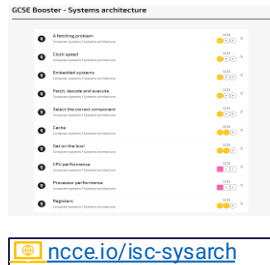
- Which parts of a computer program are held in RAM while it is processing?

- A. Only the instructions
- B. Current used Instructions and data
- C. Only the data

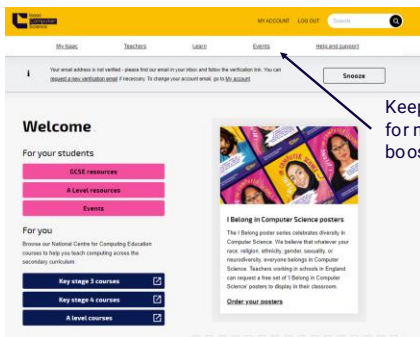


Isaac Gameboard practice

- If you want more systems architecture practice, then try this gameboard.
- You will need to sign in to **Isaac Computer Science** or register for a free account if not done already.



Check for more ISAAC boosters



Keep an eye out for more student booster events

Intended Learning Outcomes

By the end of this session, you will be able to:

- Identify the sections of the von Neumann Architecture
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Thank you