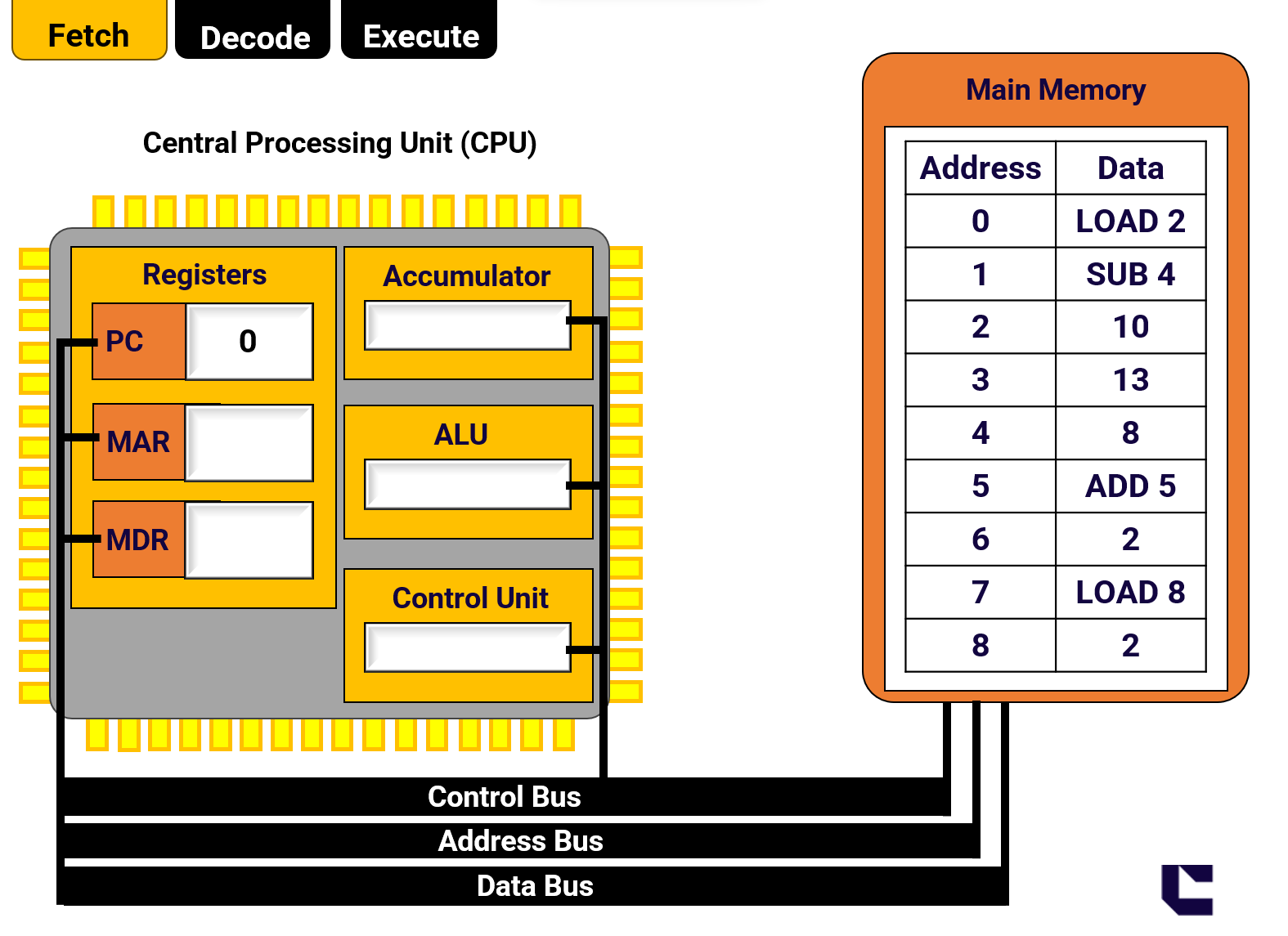
**System Architecture**

**Handout 2 – FDE Cycle**

**Task 1** - **Fetch**

Using numbers identify the correct order of steps for the **Fetch** section of the cycle?

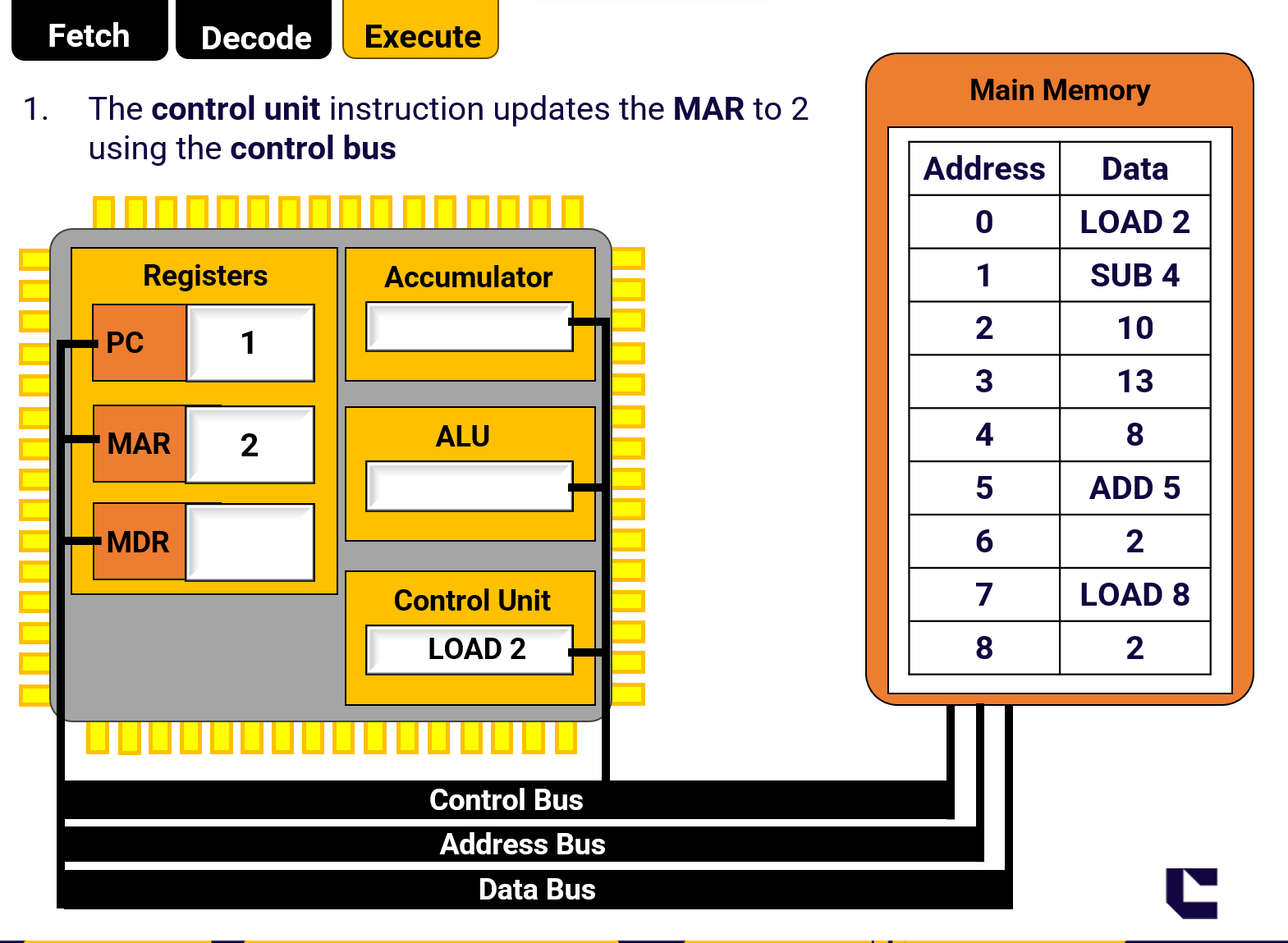


|  |  |
| --- | --- |
| **STEP order** | **Instruction** |
|  | Data held in location 0 is copied onto the data bus and transferred back to the CPU and loaded onto the MDR (Memory Data Register) |
|  | The control unit sends an instruction to the program counter to increase by 1 |
|  | MAR now holds the memory address of the next value/instruction to be fetched or stored. This is sent by the address bus to the main memory |
|  | Memory address is copied and sent on the address bus to the MAR (Memory Address Register) |

**ISAAC video for reference -** [**https://youtu.be/m6vkJV4UeI4**](https://youtu.be/m6vkJV4UeI4)

**Task 2** - **Execute**

Using numbers identify the correct order of steps for the **Execute** section of the cycle?

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|  |  |
| --- | --- |
| **STEP order** | **Instruction** |
|  | The MAR sends the instruction to the main memory along the address bus. |
|  | The control unit instruction updates the MAR to 2 using the control bus |
|  | Data held in location 2 is copied onto the data bus and transferred back to the CPU and loaded onto the MDR and stored in the Accumulator. |

**ISAAC video for reference -** [**https://youtu.be/Z3cvYfkAyOI**](https://youtu.be/Z3cvYfkAyOI)